What is claimed is:

1. A semiconductor package, comprising

a chip paddle having a thickness;

a semiconductor chip provided with a plurality of bond pads, said semiconductor chip located on an upper surface of said chip paddle; and

a plurality of internal leads formed at intervals along a circumference of said chip paddle and in electrical communication with said bond pads, said internal leads each having a thickness wherein said thickness of said chip paddle is less than said thickness of said internal leads.

2. The semiconductor package according to claim 1 wherein:

said semiconductor chip, said chip paddle and said internal leads are encapsulated by an encapsulation material.

3. The semiconductor package according to claim 1 further comprising:

at least one tie bar extending outwardly from said chip paddle, wherein said chip paddle, said internal leads and said tie bar each have a side surface and said side surface of said chip paddle, said internal leads and said tie bar are externally exposed.

4. The semiconductor package according to claim 1 further comprising:

at least one tie bar extending outwardly from said chip paddle, wherein said chip paddle, said internal leads and said tie bar each have a bottom surface and said bottom surface of said chip paddle, said internal leads and said tie bar are externally exposed.

5. The semiconductor package according to claim 1 further comprising:

a plurality of conductive wires, each of said conductive wires for electrically connecting said bond pads of said semiconductor chip to said internal leads.

6. The semiconductor package according to claim 1, wherein:

said thickness of said chip paddle is about 25-75 % of said thickness of said internal leads.

7. A leadframe for use in a semiconductor package comprising:

a chip paddle;

a plurality of inner internal leads surrounding said chip paddle and extending outwardly therefrom wherein said thickness of said chip paddle is less than said thickness of said internal leads; and

at least one tie bar in communication with and extending outwardly from said chip paddle.

8. The semiconductor package according to claim 7, wherein:

said thickness of said chip paddle is about 25-75 % of said thickness of said internal leads.

9. A method of packaging a semiconductor comprising the steps of:

providing a chip paddle having a thickness;

placing a semiconductor chip provided with a plurality of bond pads, on an upper surface of said chip paddle; and

providing a plurality of internal leads formed at intervals along a circumference of said chip paddle and in electrical communication with said bond pads, said internal leads each having a thickness wherein said thickness of said chip paddle is less than said thickness of said internal leads.

10. The method of claim 9 further comprising:

encapsulating said chip paddle, said semiconductor chip and said plurality of internal leads in an encapsulating material.

11. A packaged semiconductor comprising:

a chip paddle having a thickness;

a semiconductor chip provided with a plurality of bond pads, said semiconductor chip located on an upper surface of said chip paddle; and

a plurality of internal leads formed at intervals along a circumference of said chip paddle and in electrical communication with said bond pads, said internal leads each having a thickness wherein said thickness of said chip paddle is less than said thickness of said internal leads.